## REMARKS

Applicants would like to thank the Examiner for the thorough examination of the present application and for properly withdrawing the previous rejection. The arguments supporting patentability of the claims are presented in detail below.

## I. The Claims Are Patentable

The Examiner rejected independent Claims 12, 25, 34 and 42 over the Miyazaki et al. patent. The present invention, as recited in independent Claim 12, for example, is directed to an electronic device comprising a central processing unit, at least one peripheral device, and a data bus connected between the at least one peripheral device and the central processing unit through which data travels at a rate of a clock signal.

The electronic device further comprises a transmission line connected between the at least one peripheral device and the central processing unit for providing a random signal thereto that is synchronous with the clock signal. The central processing unit and the at least one peripheral device each comprises a data encryption/ decryption cell connected to the data bus and to the transmission line for generating a same current secret key at each clock cycle based upon the random signal.

The data encryption/decryption cell in the central processing unit and in the at least one peripheral device advantageously makes the electronic device more secure by making it more difficult to determine the data elements that travel through the data bus when an intruder observes current

consumption of the electronic device.

Independent device Claim 25 is similar to independent device Claim 12 except the at least one peripheral device has been changed to at least one memory device. Independent device Claim 34 is similar to independent device Claim 12 except this claim is directed to a smart card. Independent method Claim 42 is similar to independent device Claim 12.

Referring now to the Miyazaki et al. patent, the Examiner has taken the position that the claimed invention is disclosed in columns 7 through 9 of the Miyazaki et al. patent. The text in columns 7 through 9 corresponds to the block diagram of an IC card **101**. The IC card **101** comprises a CPU **102**, a ROM **103**, an EEPROM **104**, an I/O port **105** for controlling input/output to/from the IC card, a RAM **106**, and a residual multiplier **107**. The components are interconnected through a bus **108**.

The Applicants respectfully submit that the Examiner has mischaracterized the Miyazaki et al. patent by stating it discloses more than what is actually disclosed. First, the Examiner stated that a data bus and a transmission line are disclosed in column 7, line 58 to column 8, line 19 of the Miyazaki et al. patent. This section of Miyazaki et al. discusses the various elements in the illustrated IC card **101**, and generally refers to the bus **108**. However, no reference is made to the bus **108** comprising a data bus and a transmission line as recited in the claimed invention.

The Examiner references column 8, line 62 through column 9, line 21 as disclosing that the CPU **102** and at least one peripheral device (such as ROM **103**, EEPROM **104** and

residual multiplier **107**) comprises a data encryption/decryption cell connected to the data bus and to the transmission line for generating a same current secret key at each clock cycle based upon the random signal. The Applicants submit that Miyazaki fails to disclose a data encryption/decryption cell as recited in the claimed invention. Instead, this section in Miyazaki et al. discloses the various elliptic curve parameters used in the elliptic curve encryption processing performed with the IC card **101**.

Instead of disclosing a data encryption/decryption cell as recited in the claimed invention, a co-processor serving as a multiple length arithmetic unit is disclosed. This co-processor may be implemented by the residual multiplier **107** (column 8, lines 14-18). Reference is directed to column 9, lines 28-33, of Miyazaki et al., which provides:

> "In the flow charts referenced in the following description, it is presumed that the CPU **102** executes the programs stored in the ROM **103** while allowing the residual multiplier **107** to execute the relevant processing by using the data stored in the RAM **106** and the EEPROM **104**, as occasion requires."

Since Miyazaki et al. fails to disclose that a transmission line is connected between one of the peripheral devices and the CPU **102** for providing a random signal thereto that is synchronous with the clock signal; Miyazaki et al. also fails to disclose that the CPU **102** and one of the peripheral devices each comprises a data encryption/decryption cell connected to the data bus and to the transmission line

for generating a same current secret key at each clock cycle based upon the random signal, as recited in the claimed invention.

Accordingly, it is submitted that independent Claim 12 is patentable over Miyazaki et al. Independent Claims 25, 34 and 42 are similar to independent Claim 12. It is submitted that these independent claims are also patentable over Miyazaki et al. In view of the patentability of the independent Claims 12, 25, 34 and 42, it is submitted that the dependent claims, which include yet further distinguishing features of the invention are also patentable. These dependent claims need no further discussion herein.

In re Patent Application of:
**POMET ET AL.**
Serial No. **09/727,300**
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## CONCLUSION

In view of the arguments provided herein, it is submitted that all the claims are patentable. Accordingly, a Notice of Allowance is requested in due course. Should any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,

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## CERTIFICATE OF MAILING

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